14th Annual IEEE International ASIC/SOC Conference

The ASIC/SOC Conference, sponsored by the IEEE Circuits and Systems Society, provides a forum for sharing recent advances in VLSI/ULSI/GSI technology and design capabilities, and their application to meeting the engineering requirements for ASICs and SoCs. The 2001 Conference, sponsored by the IEEE Circuits and Systems Society offers three days of *technical papers, a poster session,* a full day of *technical workshops and Conference Banquet.*

REGISTRATION
Full Registration includes technical sessions, conference proceedings, Opening Reception and Awards Banquet. Registration for a Workshop(s) entitles the registrant to a copy of the workbook for that session.

To register, complete the enclosed Registration Form and mail or fax the form with payment to the Conference Headquarters. Advance Registration Forms must be received NO LATER THAN AUGUST 17; after August 17, you must register at the Conference and pay the late registration fee. **IEEE Members**: In order to qualify for the membership rate, you must list your IEEE membership number on the Registration Form.

Cancellations: Refund requests must be received, in writing, by August 29, 2001 in order to receive a full refund, less a $25.00 processing fee. Refund requests received after August 29 cannot be guaranteed.

HOTEL RESERVATIONS
A block of rooms has been reserved at the Hyatt Regency Crystal City. Contact the hotel directly to make a reservation, remember to identify yourself as an ASIC Conference participant.

Hyatt Regency Crystal City at Reagan National Airport
7799 Jefferson Davis Highway
Arlington, VA 22202
Reservations: 1-703-418-1234 or 1-800-233-1234
Fax: 1-703-413-6727

ASIC Conference Rates: $155 + tax for single or double room

HOTEL RESERVATIONS MUST BE RECEIVED BY AUGUST 18, 2001 TO GUARANTEE THE CONFERENCE RATE

Wednesday, September 12

PLENARY SESSION
Regency Ballroom CD - 8:30 a.m.

Opening Remarks: P.R. Mukund, General Conference Chair
Technical Program Overview: John Chickanosky, Technical Program Chair
Keynote Address: *Hiro Hashimoto, President and CEO, NEC Electronics, Inc.*
Plenary Presentations
ICs for Optical Communiction, *Prof. Behzad Razavi, University of California at Los Angeles*
HyperTransport Technology for Networking, *Peter Robinson, API NetWorks*

12:30 p.m. OPEN LUNCH

W1: LIGHT, SOUND & CYPHER
1:30 p.m. - 2:40 p.m.
Regency Ballroom C

W1.1: VLSI Implementation of High Performance Burst Mode for 128-bit Block Ciphers, Y. Mitsuyama, Z. Andales, T. Onoye* and I. Shirakawa, Osaka University, Osaka, Japan and *Kyoto University, Kyoto, Japan

W1.2: An Auditory Classifier Employing a Wavelet Neural Network Implemented in a Digital Design, J. Hughes, Rochester Institute of Technology, Rochester, NY

W1.3: Performance Evaluation of 3rd Order Sigma-Delta Modulators Via FPGA Implementation, S.S. Abeysekera and C. Charoensak, Nanyang Technological University, Singapore

W1.4: Light and Sound Data Fusion in Analog VLSI, M. Kanteti and A.H. Titus, Rochester Institute of Technology, Rochester, NY

W2: HIGH PERFORMANCE & LOW POWER CIRCUITS
1:30 p.m. - 2:40 p.m.
Regency Ballroom D

W2.1: Current-Sensing for Crossbars, M. Sinha and W. Burleson, University of Massachusetts, Amherst, MA

W2.2: Demonstration of Power Enhancements on an Industrial Circuit Through Delay Management of Non-Critical Data Paths, D. Velenis, K.T. Tang*, I.S. Kourtev**, V. Adler***, F. Baez**** and E.G. Friedman, University of Rochester, Rochester, NY, *Broadcom Corp., San Jose, CA, **University of Pittsburgh, Pittsburgh, PA, ***Sun Microsystems, Palo Alto, CA, and ****Intel Corp.

W2.3: Efficient Gate Clustering for MTCMOS Circuits, M.H. Anis, M.K. Mahmoud and M.I. Elmasry, University of Waterloo, Waterloo ON, Canada

W2.4: Gate-Diffusion Input (GDI) - A Novel Power Efficient Method for Digital Circuits: A Design Methodology, A. Morgenshtein, A. Fish* and I.A. Wagner**, Technion, Haifa, Israel, *Ben-Gurion University, Beer-Sheva, Israel, and **IBM Research Laboratory, Haifa, Israel

2:40 p.m. BREAK

W3: WIRELESS APPLICATIONS
3:35 p.m. - 4:50 p.m.
Regency Ballroom C

W3.1: ASIC and DSP Emplementation of Channel Filter for 3G Wireless TDD System, R. Veljanovski, J. Singh and M. Faulkner, Victoria University of Technology, Victoria, Australia

W3.2: A Mobile Station Modem VLSI for CDMA2000-1x, S.-C. Han, T.H. Han, Y.-C. Kim, C.-J. Kim, K.-H. Lee, I.-K. Paik, K.-H. Kim, Y.-S. Kim and S.-W. Jung, Samsung Electronics, Kyunggi-Do, Korea

W3.3: WCDMA Receiver Architecture with Unique Frequency Plan, M.A.I. Mostafa, M.C. Fernando, W.K. Chan and C. Gore, Texas Instruments, Dallas, TX

W4: SOC/IP VALIDATION I
3:35 p.m. - 4:50 p.m.
Regency Ballroom D

W4.1: Code Verification by Hardware Acceleration, H. Kohler, J. Kayser, H. Pape and H. Ruffner, IBM, Boeblingen, Germany

W4.2: Vector Language: A Proposed Verification Methodology for Intellectual Property Cores, A. Iniguez, Motorola, SPS, Tempe, AZ

W4.3: The Use of SystemC for Design Verification and Integration Test of IP-Cores, A. Fin, F. Fummi and D. Signoretto, University of Verona, Verona, Italy

4:50 p.m. - 5:30 p.m. RECEPTION
5:30 p.m. - 7:30 p.m. PANEL DISCUSSION: *Moderator: Graham Budd, ARM Limited*

Thursday, September 13

T1: WIRELESS COMMUNICATIONS
8:55 a.m. - 10:30 a.m.
Regency Ballroom C

T1.1: Algorithm, Architecture, and Implementation of Algorithmic Delay-Locked Loop Based Data Recovery Circuit for High-Speed Serial Data Communication, H. Song, Intel Corp., Chandler, AZ

T1.2: A New 246MHz Active LC Band-Pass Filter for IF Sub-Sampling GSM Receivers, M.A.I. Elmala, M.A.I. Mostafa* and S.H.K. Embabi*, Texas A&M University, College Station, TX and *Texas Instruments, Austin, TX

T1.3: A Low-Noise Fast-Settling Phase-Locked Loop with Extended Loop Bandwidth Enhancement by new Adaptation Techniques, Y. Tang, Y. Zhou*, S. Bibyk and M. Ismail, Ohio State University, Columbus, OH and *Motorola, Inc.

T1.4: On-Chip RF Filters Using Bond Wire Inductors, M.A.I. Mostafa, J. Schland and S. Lazar, Texas Instruments, Dallas, TX

T2: DIGITAL DESIGN METHODOLOGIES
8:55 a.m. - 10:10 a.m.
Potomac Room 5/6

T2.1: Direct-Mapped Asynchronous Finite-State Machines in CMOS Technology, C. Sotiriou, Foundation for Research & Technology - Hellas (FORTH), Heraklion, Crete, Greece

T2.2: A Socket Interface for GALS Using Locally Dynamic Voltage Scaling for Rate-Adaptive Energy Saving, T. Njolstad, O. Tjore, K. Svarstad, L. Lundheim, T.O. Vedal, J. Typpo, T. Ramstad, L. Wanhammar, E.J. Aas and H. Danielsen, Norwegian University of Science and Technology (NTNU), Trondheim, Norway

T2.3: MCSoC: A Platform for Clock Managed Systems on a Chip, I. Brynjolfson and Z. Silic, McGill University, Montreal, QU, Canada

T2.4: Integrated Approach to Optimized Code Generation for Heterogeneous-Register Architectures with Multiple Data-Memory Banks, S. Frohlich and B. Wess, Technische Universitat Vienna, Vienna, Austria

10:30 a.m. BREAK

T3: CIRCUIT DESIGN & APPLICATIONS
10:55 a.m. - 12:35 p.m.
Regency Ballroom C

T3.1: Input Controlled Refresh for Noise Tolerant Dynamic Circuits, A. Lakshmanan and R. Sridhar, University at Buffalo, Buffalo, NY

T3.2: A Low-Phase-Noise CMOS Ring Oscillator with Differential Control and Quadrature Outputs: L. Dai and R. Harjani, University of Minnesota, Minneapolis, MN

T3.3: A Novel All Digital Phase Locked Loop (ADPLL) with Ultra Fast Lock Time and High Oscillation Frequency, K.-H. Cheng and Y.-J. Chen, Tamkang University, Taipei Hsien, Taiwan, R.O.C.

T3.4: A Novel Impedance Control for USB2.0 Transceiver, K.-H. Koo, J.-H. Seo and J.-W. Kim, Samsung Electronics, Youngin, Korea

T4: INTERCONNECT SOLUTIONS
10:55 a.m. - 12:35 p.m.
Potomac Rooms5/6

T4.1: A Stochastic Global Net-Length Distribution for a Three-Dimensional system-on-a-Chip (3D-SoC), J.W. Joyner, P. Zarkesh-Ha and J.E. Meindle, Georgia Institute of Technology, Atlanta, GA

T4.2: A Practical Approach to DSM Repeater Insertion: Satisfying Delay Constraints while Minimizing Area and Power, A. Nalamalpu and W. Burleson*, Intel Corp., Hillsboro, OR and *University of Massachusetts, Amherst, MA

T4.3: A New Two-Layer Power/Ground Router for VLSI Layout, J.C. chi and M.C. Chi, Chung Yuan Christian University, Chung Li, Taiwan, ROC

T4.4: Estimating Interconnect Wirelength for Soft IP, P. Hung, L. Sémeria and M.J. Flynn, Stanford University, Stanford, CA

12:35 p.m. - 1:30 p.m. OPEN LUNCH

T5: PROGRAMMABLE SYSTEMS & APPLICATIONS
1:30 p.m. - 3:10 p.m.
Regency Ballroom C

T5.1: An Embedded Programmable Core for the Implementation of High Performance Digital Filters, B.I. Hounsell and T. Arslan, The University of Edinburgh, Edinburgh, Scotland

T5.2: Cell Designs for Self-Timed FPGAs, C. Traver, R.B. Reese and M.A. Thornton, Mississippi State University, Mississippi State, MS

T5.3: Reprogrammable Processing Capabilities of Embedded FPGA Blocks, T. Vaida, LSI Logic Corporation, Boulder, CO

T5.4: Low-Power Constant-Coefficient Multiplier Generator, C.-Y. Pai, A.J. Al-Khalili and W.E. Lynch, Concordia University, Montreal, Quebec, Canada

T6: LOW POWER MEMORY & CIRCUITS
1:30 p.m. - 3:10 p.m.
Potomac Rooms 5/6

T6.1: Block-Based Multi-Period Refresh for Energy Efficient Dynamic Memory, J. Kim and M.C. Papaefthymiou, University of Michigan, Ann Arbor, MI

T6.2: A Novel Low power CAM Design, G. Thirugnanam, N. Vijaykrishnan and M.J. Irwin, Pennsylvania State University, University Park, PA

T6.3: On the Low-Power Design of DCT and IDCT for Low Bit Rate Video Codecs, N. August and D.S. Ha, Virginia Tech, Blacksburg, VA

T6.4: An Improved Pass-Gate Adiabatic Logic, L. Varga, F. Kovacs and G. Hosszu, Technical University of Budapest, Budapest, Hungary

3:10 p.m. BREAK

T7: SOC/IP VALIDATION II & TEST GENERATION
3:35 p.m. - 5:15 p.m.
Regency Ballroom C

T7.1: Reuse of Addressable System Bus for SOC Testing, S. Hwang and J.A. Abraham, The University of Texas at Austin, Austin, TX

T7.2: Model Reduction Based on Value Dependency, H. Peng, Y. Moktari and S. Tahar, Concordia University, Montreal, QU, Canada

T7.3: FSimGEO: A Test Generation Method for Path Delay Fault Test Using Fault Simulation and Genetic Optimization, S. Yihe and *W. Qifa, Tsinghua University, Beijing, China and *Huawei Corporation of China, Shanghai, China

T7.4: Design Verification and DFT for an Embedded Reconfigurable Low-Power Multiplier in System-on-Chip Applications, M. Margala, X. Chen*, J. Xu*, and H. Wang*, University of Rochester, Rochester, NY and *University of Alberta, Edmonton, AL, Canada

T8: SYSTEM LEVEL DESIGN
3:35 p.m. - 5:15 p.m.
Potomac Rooms 5/6

T8.1: A Flexible Approach to the Design of Complex Embedded Systems, J.M. Moya, F. Moya and J.C. Lopez, University of Castilla-La Mancha, Ciudad Real, Spain

T8.2: Multi-Way Clustering Techniques for System Level Partitioning, M.L. Lopez Vallejo and J.C. Lopez Lopez, ETSI Telecomunicacion, Univ. Politecnica Madrid, Madrid, Spain

T8.3: A Clustering Utility Based Approach for ASIC Design, S. Areibi, M. Thompson* and A. Vannelli*, University of Guelph, Guelph, ON, Canada, *University of Waterloo, Waterloo, ON, Canada

T8.4: Structured Object Composition for System Modeling, V. Sinha, R. Gupta, University of California, Irvine, CA

4:40 p.m. - 6:00 p.m. POSTER SESSION
6:30 p.m. - 8:00 p.m. CONFERENCE BANQUET with guest speaker

POSTER SESSION

P.1: An Efficient ABR Service Engine for ATM Network, Y. Choi, S. Kang* and S. Chong**, LG Electronics, Inc., Kumi, Korea, *Yonsei University, Seoul, Korea and **KAIST, Daejon, Korea

P.2: SoC Integration of Digital Audio Applications Using Protocol Compiler and Atmel FPSLIC, K. Feske, S. Mulka, J. Schneider and G. Heinrich, FhG IIS Erlangen, Dresden, Germany

P.3: A Low Power FIR Filtering Core, A.T. Erdogan, M. Hasan and T. Arslan, University of Edinburgh, Edinburgh, Scotland

P.4: A CMOS Dual-Modulus Prescaler Based on a New Charge Sharing Free D-Flip-Flop, S.-H. Yang, K.-C. Min and K.-R. Cho, Chungbuk National University, Cheongju, Korea

P.5: Optimum Sigma-Delta De-Modulator Filter Implementation Via FPGA, S.S. Abeysekera and C. Charoensak, Nanyang Technological University, Singapore

P.6: Modular Scalable Parallel Architectures for Fast Transforms, R.W. Johnson, L.A. Koyrakh and D.M. Pihl, MathStar, Inc., Minneapolis, MN

P.7: FPGA Prototyping of a Configurable USB Device SOC, N. Balachander and S. Chonnad, Synopsys, Inc., Mountain View, CA

P.8: Network Processor Design for Optical Burst Switched Networks, P. Mehrotra, I. Baldine*, D. Stevenson* and P. Franzon, North Carolina State University, Raleigh, NC and *MCNC

P.9: Testing for AMBA(TM) Compliance, A. Nightingale, ARM IP Solutions Division, S. York, United Kingdom

P.10: IP Core Integrated and Platform Based System-On-a-Chip(SoC) Designs: An Application Perspective, T. Ramesh, IBM, Essex Junction, VT

P.11: A Comparative Cost/Performance Evaluation of Digit-Serial Multipliers for Finite Fields of Type GF(2n), G. Bertoni, L. Breveglieri and *P. Fragneto, Politecnico di Milano, Milan, Italy and *ST Microelectronics, Agrate B., Italy

P.12: A Unified Validation Methodology for System Level Co-Design and Co-Implementation, J. Goodenough, A. Bruce, A. Nightingale, P. Bates and G. Budd, ARM IP Solutions Division, S. York, United Kingdom

P.13: A VLSI Design of a High-Speed Reed-Solomon Decoder, H. Lee, Agere Systems, Allentown, PA

P.14: Dual Mode Transmitter with Adaptively Controlled Slew Rate and Impedance Supporting Wide Range Data Rates, H. Song, Intel Corporation, Chandler, AZ

P.15: Circuit Challenges and Proposed Solutions Targeting Nanometer Technologies, R.M. Secareanu, M. Jones, M. Sadd, B. White and P. Maniar, Motorola SPS, Inc., Tempe, AZ

P.16: A Dynamic Reconfigurable Clock Generator, R.M. Secareanu, D. Albonesi* and E.G. Friedman*, Motorola SPS, Inc., Tempe, AZ, *University of Rochester, Rochester, NY

P.17: SCALIP - A Scalable IP Solution for Pipelined Arrays with Limited Feedback, M. Moe and H. Schmit, Carnegie Mellon University, Pittsburgh, PA

P.18: Integrated Scheduling and Register Assignment for VLIW-DSP Architectures, T. Zeitlhofer and Bernhard Wess, Vienna University of Technology, Vienna, Austria

Friday, September 14

F1: SOC APPLICATIONS
8:55 a.m. - 10:30 a.m.
Washington A

F1.1: VLSI Reed Solomon Decoder Architecture for Networked Multimedia Applications, M. Martina, G. Masera, G. Piccinini, F. Vacca and M. Zamboni, Politecnico di Torino, Torino, Italy

F1.2: A True Block Pipelined Programmable Reed-Solomon CODEC for High-Speed/Low-Power Applications, H.-J. Kwon, J.-S. Lee, S.-H. Lee and B.-Y. Jeong, Samsung Electronics, Kyunggi-Do, Korea

F1.3: Digit-Serial Multiplier Design Using Skew-Tolerant Domino Circuits, S. Kim and G.E. Sobelman, University of Minnesota, Minneapolis, MN

F1.4: An Efficient Digit-Serial Systolic Multiplier for Finite Fields GF(2m), C.H. Kim, S.D. Han and C.P. Hong, Taegu University, Kyungbuk, Korea

F2: SOC ARCHITECTURE
8:55 a.m. - 10:30 a.m.
Washington B

F2.1: Reusable Memory Management System Design, S.K. Agun and M. Chang, Illinois Institute of Technology, Chicago, IL

F2.2: A High-Speed Multi-Port Data Buffer Design for Low-Energy DSP Applications, S. Hong, State University of New York at Stony Brook, Stony Brook, NY

F2.3: I/O Design Considerations for Multi-Application Circuits, T.L. Ruud and J.A. Wright, American Microsystems, Inc., Pocatello, ID

F2.4: Sample Integrated Fourier Transform (SIFT): A Novel Real-Time DSP Process, W.E. Pelton, T.K. Ta*, N. Yossakda**, Faster Fourier Transforms, Fremont, CA, *Fujitsu Microelectronics, Santa Clara, CA and **Northwestern Polytechnic University, Fremont, CA

10:30 a.m. BREAK

F3: COMMON SOC ISSUES
10:55 a.m. - 12:35 p.m.
Washington Room A

F3.1: CID/DRAM Mixed-Signal Parallel Distributed Array Processor, R. Genov and G. Cauwenberghs, Johns Hopkins University, Baltimore, MD

F3.2: A New Sensing and Digital-Conversion Scheme with Adaptive Image-Quality Adjustment for a Fingerprint Sensor Chip, S. Shigematsu, H. Morimura and K. Machida*, NTT Lifestyle and Environmental Technology Laboratories, Kanagawa, Japan, *NTT Telecommunication Energy Laboratories, Kanagawa, Japan

F3.3: Reducing the Cost of Scan in Deep-Sub-Micron Designs, K. Rahimi and M. Soma*, Redmond, WA and *University of Washington, Seattle, WA

F3.4: IP Protection for VLSI Designs Via Watermarking of Routes, N. Narayan, R.D. Newbould, J.D. Carothers, J.J. Rodriguez and W.T. Holman*, The University of Arizona, Tucson, AZ and *Vanderbilt University, Nashville, TN

F4: REUSE & EMBEDDED PROCESSORS
10:55 a.m. - 12:35 p.m.
Washington Room B

F4.1: Re-Useable Hardware/Software Co-Verification of IP Blocks, A. Bruce and J. Goodenough, ARM IP Solutions Division, S. York, United Kingdom

F4.2: Flexible IP Blocks for Customized Synthesis, M.M. Ziegler and M.R. Stan, University of Virginia, Charlottesville, VA

F4.3: Design Methods for System-On-A-Chip Control CODECs to Enhance Reuse, J.S. Fisher and S.B. Bibyk, Ohio State University, Columbus, OH

F4.4: A Hierarchical Simulation Framework for Application Development on System-on-Chip Architectures, V. Mathur and V.K. Prasanna, University of Southern California, Los Angeles, CA

12:35 p.m. - 1:30 p.m. OPEN LUNCH

F5: PHYSICAL DESIGN, ALGORITHMS & SIMULATION
1:30 p.m. - 2:25 p.m.
Washington Room A

F5.1: Noise-Aware Synthesis of Electrostatic Discharge Networks in Mixed-Signal Integrated Circuits, J. Lee, Y. Huh*, P. Bendix* and S.-M. Kang**, University of Illinois, Urbana, IL, *LSI Logic Corp., Milpitas, CA, and **University of California, Santa Cruz, CA

F5.2: A Global Routing Methodology for Analog and Mixed-Signal Layout, K. Sajid, J.D. Carothers, J.J. Rodriguez and W.T. Holman, The University of Arizona, Tucson, AZ

F5.3: Evaluating the Impact of Architectural-Level Optimizations on Clock Power, D. Duarte, V. Narayanan, M.J. Irwin and M. Kandemir, The Pennsylvania State University, University Park, PA

F6: ADC & SWITCHED CURRECT CIRCUITS
1:30 p.m. - 2:50 p.m.
Washington Room B

F6.1: Future-Ready Ultrafast 8bit CMOS ADC for System-on-Chip Applications, J. Yoo, D. Lee, K. Choi and A. Tangel*, The Pennsylvania State University, University Park, PA and *University of Kocaeli, Yzmit, Turkey

F6.2: A Low-Power Variable Resolution Analog-To-Digital Converter, C. Aust, R.S. Richmond* and D.S. Ha*, IBM Microelectronics, Research Triangle Park, NC and *Virginia Tech, Blacksburg, VA

F6.3: A Low-Voltage Switched-Current Memory Cell Based Delta Sigma Modulator, A.S. Botha, P. Sniatala, K.W. Hsu and P.R. Mukund, Rochester Institute of Technology, Rochester, NY

F6.4: Low-Voltage Switched-Current Circuits for Mixed Signal Systems, A. Handkiewicz, M. Lukowiak and M. Kropidlowski, Poznan University of Technology, Poznan, Poland

TUTORIAL WORKSHOPS

MORNING WORKSHOPS
September 15, 2001, 8:00am – 12:00pm

TW1: An Introduction to Bluetooth: A Standard for Short-range Wireless Networking, *Prof. Dennis Sweeney, Virginia Tech Center for Wireless*
Bluetooth is an emerging standard for short-range low-cost wireless connectivity for consumer devices and Personal Area Networks (PAN). It is a frequency hop spread spectrum system intended for worldwide operation in the unlicensed 2.45 GHz Industrial Scientific Medical (ISM) band. Bluetooth is more than just a radio; it is an entire networking standard. This tutorial will provide a look under the "logo" at the basic structure of Bluetooth, its capability to transmit both voice and data, and its software "stack." It will also examine interference issues and some of the resources available for developing Bluetooth applications.

Prof. Sweeney is with the Center for Wireless Telecommunications (CWT) at Virginia Tech. His interests are in unlicensed wireless applications, Local Multipoint Distribution Services (LMDS), and radio frequency circuit design. He directs the CWT's RF Design Lab. This lab has been involved in the design of 900 MHz spread spectrum communications system and a 3-G test bed radio. In addition to RF circuit design, Dr. Sweeney's interests include microwave propagation including satellite slant path propagation and propagation for wireless applications. His current project is a short pulse channel sounder for LMDS. Dr. Sweeney worked on Global Positioning System (GPS) receiving equipment and applications at the Jet Propulsion Laboratory in Pasadena, CA. He teaches both undergraduate and graduate courses in Radio Engineering, electronics and satellite communications, and short courses on filter design and unlicensed wireless.

TW2: SoC Signal Integrity and Power Delivery Design Challenges and Solutions, *Prof. Charlie Chen, University of Wisconsin*
This tutorial presents signal integrity and power delivery design challenges and possible solutions for high-speed, low power, deep sub-micron, and millions-of-transistors SoC VLSI design. Starting from technology scaling trends, several signal integrity issues such as capacitance and inductance modeling, electrical and magnetic coupling noises, and their impacts to timing will be discussed. Novel signal integrity analysis algorithms, optimization methods, and design methodology will be presented. Power delivery issues such as IR drop, Ldi/dt drop, and packaging resonance problems will also be discussed in detail. Several comprehensive power delivery design methodology and efficient analysis techniques will also be presented.

Charlie Chung-Ping Chen received his B.S degree in computer science and information engineering from the National Chiao-Tung University, Hsinchu, Taiwan, in 1990 and his M.S. and Ph.D. degrees in computer science from the University of Texas at Austin in 1996 and 1998. From 1997-1999 he was with Intel Corporation as a senior CAD engineer with Strategic CAD Labs. He was in charge of several interconnect and circuit synthesis projects in the micro-processor group. Currently, he is an assistant professor in the ECE Department at the University of Wisconsin, Madison. His research interests are in the areas of computer-aided design and microprocessor circuit design with an emphasis on interconnect and circuit optimization as well as signal integrity analysis and optimization. Prof. Chen received the D2000 award from Intel Corp. and National Sciences Foundation Faculty Early Career Development Award (CAREER) at 1999 and 2001, respectively.

AFTERNOON WORKSHOPS
September 15, 2001, 1:00pm – 5:00pm

TW3: Low-Voltage Current-Mode Analog Circuit Structures and Applications, *Prof. Sudhanshu Jamuar, Indian Institute of Technology, New Delhi, India*

This tutorial presents an overview of techniques used for low-voltage, low-power analog circuit structures. Brief details of prevalent techniques such as bulk-driven transistors, sub-threshold transistors, and level shifter transistors will be presented along with their merits and demerits. Advanced current mirrors and voltage buffers, signal processing cells, and applications in analog signal processing and other specialized signal processing applications are explored in detail.

Prof. Sudhanshu Jamuar received his PhD from the Indian Institute of Technology, Kanpur, India, in 1977. Since 1977, he has been with the Indian Institute of Technology, New Delhi, where he is presently a full professor and leads research on analog/digital circuits and communication systems. He is a Fellow of the Institute of Electronics and Telecommunications, India.

TW4: Low-noise Systems on Chip for 3G Wireless, *Dr. Sam Martin and Dr. Michael Heutmaker, Bells Labs, Lucent Technologies*

This workshop addresses issues of strong current interest in developing high performance SoC devices for wireless applications. An overview of system aspects of wireless voice/data communications, highlighting 3G/4G cellular is provided. Trends in the development of 3G wireless communication systems will be discussed with emphasis on low noise SoC design challenges, such as DC to RF migration, mixed-signal and noise interference/substrate cross-talk issues.

Samuel Martin received his M.S. and Ph.D. Degrees in Condensed Matter Physics from the University of Frankfurt in West Germany and then joined AT&T Bell Labs in 1987. He is presently a distinguished member of technical staff in the Semiconductor Physics Research Department at Bell Laboratories, Lucent Technologies in Murray Hill, NJ. He has worked on developing low frequency flicker noise measurement methods and on measurements and modeling of RF noise properties of various semiconductor device technologies used in wireless applications. He is presently involved in the RFIC integration of next generation base station products. He holds six patents and has contributed to over 60 publications as well as to over 50 technical talks.

Michael Heutmaker joined Lucent Technologies (then AT&T) in 1986 after receiving a Ph.D. in Physics from the University of Pennsylvania. He has worked in wireless test and product development since 1990, and presently specializes in the measurement and analysis of digitally-modulated signals in wireless systems and circuits. Mike holds six patents and has published approximately 15 papers. Since 1997 he has been Technical Program Chair and/or General Chair of the IEEE Radio and Wireless Conference (RAWCON).

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